Ohio University
Department of Electrical Engineering and Computer Science
Term Paper for EE 561A Fall 2008
8 October 2008

The term project for this quarter is an independent study on a selected area of high-performance computing (HPC). It requires reading of research literature, analysis of existing or proposed techniques, and some synthesis of new ideas. You should select only one sub-topic area from the list attached for an in-depth study and submit an investigation report. Your investigation should be based on up-to-date information through scientific journals, conference proceedings, high-tech and trade magazines, technical manuals supplied by manufacturers, etc. Do not just make a list or summary of existing references on a particular area.

A professionally documented report is required. The report should be technically informative and highly written (it must be typed). There is no page limit on the report (anywhere from 15 printed single-space pages to 30 is fine). Each person is expected to turn in his own report. Your work should be done individually and independently; no collaboration is allowed except for sharing references.

General Guidelines

1. You should select your sub-topic from the list attached.

2. Submit to me by October 15, 2008 a brief one-page written project proposal containing the following information:
   - submit a one paragraph statement of the problem that you will investigate,
   - the significance of the problem and its relationship to HPC and the main topic,
   - a proposed plan of research, including your approach and expected results (impact of your research on the problem),
   - A list of the most recent publications about the project that you have gathered so far.

3. Turn in your final complete typed report no later than Nov 14, 2008. This is a firm deadline. It should have:
   - an abstract describing the nature of the work, an introduction,
   - a detailed analysis of the subject area and the major results obtained,
   - conclusions, references, and possibly, although not required, future work to be done in that area (just some suggestions, in case someone else wants to expand your work). References should be written according to the IEEE format (see any IEEE published paper for an example).
Milestone Dates

- **October 8, 2008**: Project is assigned to each student.
- **Oct 15, 2008**: Project proposal is due.
- **Nov 14, 2008**: Term paper is due. Please submit a hardcopy of the term paper and drop it in my mailbox (Avinash Kodi). If it is not possible, send the softcopy of the paper to avinashk@eecs.ohio.edu.

Sources of Information

Let me first tell you how to go by getting the appropriate reference to start your project.

1. A couple of good survey papers to start with are:
   - On-Chip Network Bibliography: http://www.cl.cam.ac.uk/~rdm34/onChipNetBib/browser.htm
   - Workshop on On-Chip Networks http://www.ece.ucdavis.edu/~ocin06/

2. There are also several books on the subjects. You may see me if you need more sources.
   - Principles of Interconnection Networks By William Dally and Brian Towles
   - Networks on Chips: Technology and Tools (Systems on Silicon) By Giovanni De Micheli and Luca Benini
   - Networks on Chip By Axel Jantsch and Hannu Tenhunen
   - System-on-Chip: Next Generation Electronics (Circuits, Devices and Systems) By Bashir M. Al-Hashimi
   - Multiprocessor Systems-on-Chips (Systems on Silicon) By Ahmed Jerraya and Wayne Wolf
   - Interconnection Networks, an Engineering Approach By Jose Duato, Sudhakar Yalamanchilli and Lionel Ni
   - Interconnection Networks for Large-Scale Parallel Processing By Howard Jay Siegel
   - Interconnection Networks for Multiprocessors and Multicomputers: Theory and Practice By Anujan Verma and C.S.Raghavendra
   - Introduction to Parallel Algorithms and Architectures: Arrays, Trees, Hypercubes By F. Thomson Leighton
   - Parallel Computer Architecture, A Hardware/Software Approach By David E. Culler
   - Jaswinder Pal Singh with Anoop Gupta
3. Other journals to look at are:
   - IEEE Transactions on Parallel and Distributed Systems.
   - IEEE Transactions on Computers.
   - IEEE Computer, IEEE Micro, IEEE Design and Test
   - IEEE Parallel and Distributed Technology
   - Proceedings of the IEEE
   - Journal of Parallel and Distributed Computing
   - IEEE Network
   - The Computer Journal.
   - Communications of the ACM (Association of the Computing Machinery).

**Term Paper Topic: Network-on-Chips (NoCs)**

Chip design has four distinct aspects: computation, memory, communication, and I/O. As processing power has increased and data intensive applications have emerged, the challenge of the communication aspect in single-chip systems, Systems-on-Chip (SoC), has attracted increasing attention. A prominent concept for communication in SoC is known as Network-on-Chip (NoC). Network-on-chip (NoC) research addresses global communication in SoC, involving (i) a move from computation-centric to communication-centric design and (ii) the implementation of scalable communication structures.

The scaling of microchip technologies has lead to a doubling of available processing resources on a single chip every second year. Even though this is projected to slow down to a doubling every three years in the next few years for fixed chip sizes [ITRS 2003], the exponential trend is still in force. Historically, computation has been expensive and communication cheap. With scaling microchip technologies, this changed. Computation is becoming ever cheaper, while communication encounters fundamental physical limitations such as time-of-flight of electrical signals, power use in driving long wires/cables, etc. In comparison with off-chip, on-chip communication is significantly cheaper. There is room for lots of wires on a chip. Thus the shift to single-chip systems has relaxed system communication problems. However on-chip wires do not scale in the same manner as transistors do, and the cost gap between computation and communication is widening. Meanwhile the differences between on- and off-chip wires make the direct scaling down of traditional multicomputer networks suboptimal for on-chip use.

In this term paper, you will work on the design, analysis, and performance of on-chip networks. You will have to choose from the following sub-topics:

**List of Sub-Topics**

1. On-Chip Photonic Networks
2. Routing, Switching and Flow Control in NoCs
3. Cache Coherence Optimized NoCs