Section 1: HARDCOPY SUBMISSION (100 Points)

1. **(20 Points)** Here is a series of address references given as word addresses: 2, 3, 11, 16, 21, 13, 64, 48, 19, 11, 3, 22, 4, 27, 6 and 11. Assuming a direct-mapped cache with 16 one-word blocks that is initially empty, label each reference in the list as a hit or miss and show the final contents of the cache.

2. **(20 Points)** Show the hits and misses and final cache contents of a direct-mapped cache with four-word blocks and a total size of 16 words.

3. **(20 Points)** Compute the total number of bits required to implement the cache in Figure 5.9 on page 469. This number is different from the size of the cache, which is usually refers to the number of bytes of data stored in the cache. The number of bits needed to implement the cache represents the total number of memory needed for storing all the data, tags and valid bits.

4. **(20 Points)** Consider the 3 processors with different cache configurations
   a. Cache 1: Direct-mapped with one-word blocks
   b. Cache 2: direct-mapped with 4-word blocks
   c. Cache 3: Two-way set associate with 4-word blocks

   The following are the miss rates
   a. Instruction miss rate is 4% and data miss rate is 6%
   b. Instruction miss rate is 2% and data miss rate is 4%
   c. Instruction miss rate is 2% and data miss rate is 3%

   For the processors, one-half of the instructions contain a data reference. Assume that the cache miss penalty is 6 + Block size in words. The CPI for this workload was measured on a processor with cache 1 and was found to be 2.0. Determine which processor spends the most cycles on the cache miss.

5. **(20 points)** If the cache access time determines the processor’s clock cycle time, which is often the case, AMAT may not correctly indicate whether one cache organization is better than another. If the processor's clock cycle time must be changed to match that of a cache, is this a good trade-off? Assume the processors are identical except for the clock rate; assume 1.5 references per instruction and a CPI without cache misses of 2. The miss penalty is 20 cycles for both processors.

   (a) What is the AMAT for the original machine with a 500 MHz clock which takes a 1 clock cycle for cache hit with a miss rate of 5%?

   (b) What is the AMAT for the new machine that doubles the cache size to reduce the miss rate to 3% but causes the hit time to increase by 20%?

   (c) What is the impact on the execution time if the new hit time is the clock cycle time?