Preliminary Questions for Working Group 2: Nanophotonics Technology Architecture

Integration strategies

1. Backend extension for bulk (Intel 2009, Cornell) - SiN on CMOS die, how to make good active devices - early polySi examples Cornell and electro-optic modulators (Intel) - drive voltages too high for underlying CMOS? - How to scale them down.

2. Monolithic integration (balance the cost of process development with energy/bit of the electrical backend in a given node) - e.g. if process costs nothing like MIT approach, want most advanced process in which photonics can be built to lower energy/bit and increase bandwidth density - broadens the set of applications where this can be used. If new process developed - want to stay in potentially older nodes for longer reach comm since pressure on bw density and energy/bit not too high (extreme example - active cables - Luxtera).

3. Challenge for photonics - how to do monolithic beyond 22nm? Not even transistor people know what will happen - perhaps an opportunity for two camps to start talking...

4. Do TSV approaches with photonics-only plane have any chance? Unpredictable parasitic caps at Rx and impact on laser power which is very precious.

Prototyping and Relevance

1. Need prototypes with larger number of devices to address systems/link issues and enable architects to do good modeling across the stack. Also enables device people to realize highest design sensitivities and where they can be handled (process, device, circuit or system level)

2. Relevance gap 100k (arch) vs. 10 devices (prototypes) - need to meet in the middle to transition from Honeymoon (idealized arch studies) to Realization period (architectures that work despite realistic issues).

Network on chip and System perspective

1. Is Coherency needed?
   - MPI vs. Shared memory model (2-10x code write-time improvement for SM) provided there is hardware NoC to carry it out.
   - For enterprise (Google, Facebook) already use distributed arch – so what's the point for shared memory (scale 1M nodes). But what happens in 100-1000 cores regime.

2. Can the optics help with simplifying the core architecture (# of outstanding requests) that result from deepening of the electrical NoC cache hierarchy for electrical NoC – i.e. get more energy-efficient system by not only imporving the energy of optical NoC, but helping simplify the cores as well (since cores still most dominant energy cost).

3. Macro Instructions for networks (analogous to computation with accelerators). Programmable/Reconfiguration network. Is that hard to program?

4. Scaling performance - only way to do it is to scale on-chip radix -need hierarchy in network (a blessing and a curse). Software people can't worry about locality as they try hard to parallelize the programs.

5. Can optics help with extreme low-power handheld? Largest pressure for efficient compute hardware, at the same time creates the earliest push for energy-efficient on-chip/off-chip interconnect. What can we do in a couple of Watts in next 10 years? How can optics help?