Course Syllabus
Spring 2018 EE 4683/5683: Computer Architecture

Course Information
Credits: 3
Days: W
Time: 12:55 - 1:50 PM
Location: ARC 321
Webpage: http://oucsace.cs.ohiou.edu/~avinashk/classes/ee468/ee468.htm

Course Instructor Information
Name: Avinash Kodi
Rm: STKR 322D
Phone: (740)-597-1481
E-mail: kodi@ohio.edu
Office Hours: 10:00 PM - 2:00 PM (Wednesday), or by appointment

Grading Assistant
Name: TBD
Rm: TBD
E-mail: TBD
Office Hours: TBD

Textbook

Prerequisites
- EE 3613: Computer Organization

Class Policies
- Class Meeting: As this is an online class, there will be no regular meeting as all instructional screencasts, lecture notes and assignments will be posted online. However, for the convenience of the students (undergrads and grads), I will periodically meet with the students, every 2-3 weeks to discuss the critical issues with the class. The time and location will be chosen so that it is convenient for the majority of the students and all students will be informed via email before any such meeting.

- Lectures: There are a total of 7 modules with multiple sub-parts covering computer architecture topic. Each module will be composed of lectures slides (PDFs) and instructional screencasts (voice-over powerpoint slides). These will be posted on a weekly basis and students will be notified via email. All lecture slides will be posted on the course website; the instructional screencasts will be available via blackboard. Each screencast will be 10 - 20 minutes and will be accompanied with powerpoint slides. Since this is an online course, it is up to you to keep up with the lessons, readings and assignments. This is critical since much of the material builds on itself and if you get a few weeks behind, it can be extremely difficult to catch up.
• **Assignment Submission**: All assignment submissions are due according to the due dates indicated in the course schedule. Periodically, I will send reminders when they become due. All assignments will be collected via blackboard.

• **Exam Submission**: For all students registered for the class, there will be in-class exam midterm and final exam scheduled. The exam will be regular paper-and-pencil exam where the midterm will be one hour and the final will be two hours.

• **Make-Up Exam**: Make-up exams will only be given to those with valid university absences such as documented illness. In such cases, the student is to contact the instructor as soon as is practicable to schedule a make-up exam.

• **Academic Misconduct**: Any academic dishonesty will not be tolerated. Unless otherwise specifically stated by your instructor, all course work should be done on your own. Please refer to the OU Student Code of Conduct.

• **Regrades**: All requests for regrades must be submitted in within one week of the distribution of the graded material.

• **Late Homeworks**: Late homework assignment will be accepted for a maximum of four days after the due date. For each day your assignment is late, 10% of the total possible points will be deducted from your score.

**Undergraduates/Graduates Grading Policy**

- Homeworks (4): 20%
- Midterm (1): 25%
- Final Exam: 30%
- Projects (2): 25%

• Assignments are due via e-mail or through Blackboard on the date and time specified.

• All grades will be posted on Blackboard.


• All exams will be closed book and closed notes.

**Course Outline**

EE 4683/5683 is intended to provide undergraduate and graduate students with an in-depth study of digital systems and computer design. It provides a basic knowledge and ability required for understanding and designing computer systems. The important topics covered in this class include cache and main memory concepts, virtual memory, multi-level caches, I/O devices, multiprocessor networks, snoopy and directory cache coherence. Graduate students are expected to complete a term-paper. The topics covered in this course are as follows:

• Performance Trade-offs for Multicores

• Advanced Pipelining: Superscalar and VLIW

• Instruction Level Parallelism: Static and Dynamic Scheduling

• Limits to ILP: Multithreading and Multicores

• Memory Hierarchy and Multi-Level Caching
• I/O Fundamentals and Techniques
• Shared Memory Multiprocessing
• Interconnection Networks & Clusters

**Student Outcomes vs. Course Learning Outcomes**

**A: An Ability to Apply Knowledge of Math, Science and Engineering**

• Ability to understand the factors that contribute to computer performance.
• Ability to understand the limitations of performance metrics.
• Ability to understand the basic components of the processor pipeline.
• Ability to understand pipelining, Instruction Level Parallelism (ILP), hazard detection and the limitations of ILP.
• Ability to understand the effect on memory latency and bandwidth on performance.
• Ability to understand the performance trade-offs in designing the main memory.
• Ability to understand the principles of memory management
• Ability to understand the working of I/O devices that assist in transferring information from memory, network, hard disk to/from the processor.
• Ability to understand the design trade-offs in multiprocessor based cache coherent snoopy systems, which are common nowadays in multi-core architectures.
• Ability to understand distributed cache coherence in multiprocessor systems.
• Ability to understand the underlying network characteristics used for communication.

**B: Design and Conduct Experiments, Analyze and Interpret Data**

• Ability to understand the language of the computer: Instruction Set Architecture and program using the same.
• Ability to understand various trade-offs among various cache organizations.

**Tools**

• *WinMIPS64* - MIPS64 instruction set simulator for Windows
• *Dinero* - Cache simulator runs on Unix, linux or Cygwin

**Tentative Dates**

• Midterm Exam: Wednesday March 7, in-class
• Final Exam: Monday April 30, from 4:40 PM - 6:40 PM.