

Department of Electrical Engineering and Computer Science
Ohio University, Athens, Ohio.

Course Syllabus
Winter 2012 EE 467/567: Advanced Microprocessors

Course Information

Credits: 3

Days: MWF

Time: 3:10 - 4:00 PM

Location: Academic Research Center (ARC) 212

Webpage: <http://oucsace.cs.ohiou.edu/~avinashk/classes/ee467/ee467.htm>

Course Instructor Information

Name: Avinash Kodi

Rm: STKR 322D

Phone: (740)-597-1481

E-mail: kodi@ohio.edu

Office Hours: 10:00 AM - 12:00 PM (Monday and Wednesday) or by appointment

Textbook/Reference Materials

- (*Required*) "The Intel Microprocessors," 8th edition, by Barry B. Brey, ISBN-10: 0-13-502645-8, ISBN-13: 978-0-13-502645-8
- "IA-32 Intel Architecture Software Developer's Manual Volume 1: Basic Architecture," Intel Corporation
- "IA-32 Intel Architecture Software Developer's Manual Volume 2a: Instruction Set Reference, A-M," Intel Corporation
- "IA-32 Intel Architecture Software Developer's Manual Volume 2a: Instruction Set Reference, N-Z," Intel Corporation
- "IA-32 Intel Architecture Software Developer's Manual Volume 3: System Programming Guide," Intel Corporation
- "The Intel Microprocessors - Architecture, Programming, and Interfacing," Barry B. Brey, Prentice-Hall.
- "Modern Processor Design - Fundamentals of Superscalar Processors," John Paul Shen, Mikko H. Lipasti, Mc Graw Hill.
- "NASM - The Netwide Assembler - Version 0.98.34"
- "The 8088 and 8086 Microprocessors - Programming, Interfacing, Software, Hardware, and Applications," Third or Fourth Edition, Walter A. Triebel and Avtar Singh
- "The 80x86 IBM PC and Compatible Computer (Volumes I & II) - Assembly, Language, Design, and Interfacing," Fourth Edition, Muhammad Ali Mazidi, Janice Gillispie Mazidi, Prentice-Hall

- Computer Architecture - A Quantitative Approach, John L. Hennessy and David A. Patterson, 4th Edition.
- Computer Organization and Design - The Hardware/Software Interface, David A. Patterson and John L. Hennessy, 3rd Edition.

Prerequisites

- EE 395A, permission or CpE option

Class Policies

- *Attendance:* Class attendance is strongly encouraged. Please note that while textbook is a reference, many handouts and problems will be discussed in class.
- *Academic Misconduct:* Any academic dishonesty will not be tolerated. Unless otherwise specifically stated by your instructor, all course work should be done on your own. Please refer to the OU Student Code of Conduct.
- *Reading:* Be prepared. Read over the material before class. I will do my best to post upcoming lecture topics. Check the class webpage regularly for announcements.
- *Regrades:* All requests for regrades must be submitted in within one week of the distribution of the graded material.
- *Late Homeworks:* Late homework assignment will be accepted for a maximum of two days after the due date. For each day your assignment is late, 25% of the total possible points will be deducted from your score.

Undergraduates Grading Policy

Homeworks (4): 15%
 Midterm : 20%
 Final Exam : 30%
 Projects (2) : 35%

Graduates Grading Policy

Homeworks (4): 15%
 Midterm : 20%
 Final Exam : 25%
 Projects : 20%
 Term Paper : 20%

- Assignments are due in class, via e-mail or through Blackboard on the date and time specified.
- All grades will be posted on Blackboard.
- All grading is based on the 12-point system. [100-93] A, [92-90] A-, [89-87] B+, [86-83] B, [82-80] B-, [79-77] C+, [76-73] C, [72-70] C-, [69-67] D+, [66-63] D, [62-60] D-, [59-..] F. Instructor reserves the right to lower the limits above, but I promise not to raise them.
- All exams will be closed book and closed notes.

Tentative Dates

Midterm: Wednesday Feb 1, 2012 (in-class)

Last day to drop Class: Monday Feb 6, 2012

Term Paper Due: March 16, 2012

Final Exam: Monday March 12, 2012 (12:20 - 2:20 PM)

Course Outline

The course is focused on the organization of 16- and 32-bit microprocessors. Particular attention is given to the 8086 family (8086/286/386/486/Pentium I-IV) regarding instruction set, assembly language programming, arithmetic operations, computer architectural features, memory hierarchy, I/O interfacing, floating-point unit, and various other topics. Furthermore, comparisons will be made to other microprocessors such as the PowerPC family of microprocessors.

Course Outcomes

- An ability to understand the basic components of a microprocessor pipeline.
- An ability to understand the software architecture and the instruction set architecture (ISA) of the Intel 16-bit and 32-bit architectures (IA32).
- An ability to understand the addressing modes and basic parts of an assembly instruction.
- An ability to use the ISA of the IA32 to write programs for an Intel machine using the Netwide Assembler (NASM).
- An ability to understand the real-mode and protected-mode operation of the IA32.
- An ability to understand cache memories.
- An ability to understand the manner in which the microprocessor is interfaced to memory components.
- An ability to understand the manner in which the microprocessor is interfaced with Input/Output (I/O) components.
- An ability to understand the basic operation of the IA32 and IA64 microprocessor cores.