Course Information
Class Number: 2648
Section: 100
Credits: 3
Days: MWF
Time: 2:00 - 2:55 PM
Location: ARC 321
Webpage: http://oucsace.cs.ohiou.edu/~avinashk/classes/ee461a/ee461a.htm

Course Instructor Information
Name: Avinash Kodi
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Teaching Assistant Information
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Office Hours: Mon and Wed 3:00 - 5:00 PM or by appointment

Textbook

Prerequisites
• EE 1024: Introduction to Computer Engineering
• CS 2400: Programming in C

Class Policies
• Attendance: Class attendance is strongly encouraged. Please note that while textbook is a reference, many handouts and problems will be discussed in class.
• Laptop/Smartphone: Students are strongly encouraged to use laptops/smartphones during lectures, however the content must be related to the course only.
• Academic Misconduct: Any academic dishonesty will not be tolerated. Unless otherwise specifically stated by your instructor, all course work should be done on your own. Please refer to the OU Student Code of Conduct.
• **Reading:** Be prepared. Read over the material before class. For the most part lecture will follow mostly the organization of the book. I will do my best to post upcoming lecture topics. Check the class webpage regularly for announcements.

• **Regrades:** All requests for regrades must be submitted in writing within one week of the distribution of the graded material.

• **Late Homeworks:** Late homework assignment will be accepted for a maximum of two days after the due date. For each day your assignment is late, 25% of the total possible points will be deducted from your score.

Undergraduates Grading Policy

Homeworks (5): 20%
Midterms (2) : 30%
Final Exam : 30%
Project : 20%

• Assignments are due in class, via e-mail or through Blackboard on the date and time specified.

• All grades will be posted on Blackboard.


• Exams can be either be closed book or open book. Precise instructions will be provided before each exam.

• **Undergraduates:** All project related work should be done in pairs. This is gradually built during the course of the semester.

**Course Outline**

EE 3613 is intended to provide undergraduate students with an in-depth study of computer organization. It provides a basic knowledge and ability required for understanding and designing standard and novel computer systems. The important topics covered in this class include

• Amdahl’s Law and Performance
• Instruction set architecture (ISA)
• Arithmetic for computers
• The Processor: Datapath and Control
• Enhancing Performance with Pipelining
• Cache and Main Memory Concepts
• I/O Devices and Storage

**Student Outcomes vs. Course Learning Outcomes**

A: An Ability to Apply Knowledge of Math, Science and Engineering
• Ability to understand the performance trade-offs in designing computers.
• Ability to understand how the basic components of the processor pipeline works.
• Ability to understand various trade-offs among instruction set architectures.
• Ability to understand how computers perform basic arithmetic.
• Ability to understand the design and working of the processor’s data and control system.
• Ability to understand the design trade-offs in various cache and main memory organizations.

B: Design and Conduct Experiments, Analyze and Interpret Data
• Ability to understand the language of the computer: Instruction Set Architecture using QtSPIM.
• Ability to understand the design of processor pipeline using Verilog.

Tools
• SPIM (now called QtSpim, an assembly level language programming tool
• Verilog, for logic synthesis and ISA implementation

Project (Undergrad)
The requirements for final project are (done in groups of 2):
• Design an instruction set (Done as a part of an assignment)
• Implement this instruction set using a pipelined data path.
• Each module should be separately testable (Mostly has been done in part as assignments).
• Integrate the modules as one unit and test it out.
• Write a small program that can be easily modified (either one or two instruction or data part)
• Write a report that details the following: purpose of the processor, instruction set definition, instruction format, design methodology, description of the modules and testing methodology.

Tentative Schedule
• Week 1: Chapter 1 CPU Performance and Evaluation
• Week 2-3: Chapter 2 Instruction Set Architecture, SPIM tutorial
• Week 4-5: Chapter 3 Computer Arithmetic
• Week 6: Logic Design and Full Adders, Verilog
• Week 7-8: Chapter 4 Processor: Control and Data Path
• Week 9-12: Chapter 4 Pipelining
• Week 12-14: Chapter 5 Cache and Main Memory
• Week 15: Chapter 6 Storage and I/O

Tentative Dates
Midterm 1: Wednesday February 15, 2017 (in-class)
Midterm 2: Friday April 7, 2017 (in-class)
Project Due: Friday April 21, 2017
Final Exam: Monday April 24, 2017 (12:20 - 2:20 PM)