Course Syllabus
Fall 2010 EE 224: Introduction to Digital Circuits & Computer Design

Course Information
Credits: 4
Class Location: Grover E 218
Class Days: M,W
Class Time: 10:10 - 12:00 PM
Lab Location: Stocker Engineering Building STKR 306
Lab Day: T
Lab Time: 10:10 - 12:00 PM

Course Instructor Information
Name: Avinash Kodi
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Phone: (740)-597-1481
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Webpage: http://oucsace.cs.ohiou.edu/~avinashk/classes/ee224/ee224.htm
Office Hours: 3:00 PM - 5:00 PM Monday, 8:00 AM - 10:00 AM Wednesday or by appointment

Textbook

Prerequisites
- EE 103

Class Policies
- **Attendance:** Class attendance is required. If you will need to miss class for some reason, you should contact your instructor in advance to determine the consequences of missing class. Please note that while textbook is a reference, many problems and exercises will be discussed in class.

- **Academic Misconduct:** Any academic dishonesty will not be tolerated. Unless otherwise specifically stated by your instructor, all course work should be done on your own. Any exceptions to this could result in an "F" for the course. Please refer to the OU Student Code of Conduct.

- **Reading:** Be prepared. Read over the material before class and laboratory. For the most part lecture will follow mostly the organization of the book. I will do my best to post upcoming lecture topics, when necessary. Check the class webpage regularly for announcements.
• **Homeworks:** Homework exercises will be assigned weekly throughout the term to assist you in mastering the basic course concepts. It is strongly encouraged that any student having difficulty with homework assignments come to office hours or email the instructor with questions. No late homework assignments will be accepted. Please contact the instructor in case of emergencies.

• **Quizzes:** There will be at least 2-3 in-class pop quizzes in this course. These will be both open and closed book quizzes. There will be no makeup quizzes.

• **Exams:** We will have three exams (two Midterms and one Final) in this course to give you the opportunity to show that you have mastered the knowledge and skills addressed. Two midterm exams have the same weight and cover roughly two halves of the course work, while the final exam is based on all classwork including the lab modules.

• **Laboratory:** The teaching assistant for EE 224 for the Spring 2010 quarter is Mr. Xinming Yu, a graduate student in the EECS department ([xy188005@ohio.edu](mailto:xy188005@ohio.edu)). In the laboratory you will be expected to record your observations and results on prepared lab sheets. *Students must inform the instructor ahead of time regarding absence from lab when possible, and all missed labs must be made up by the end of the following week.* All lab write-ups are due the following week during the regular lab session.

**Grading Policy**

Homeworks and Quizzes : 15%
Midterms (2) : 40%
Final Exam : 20%
Projects : 25%

• All grades will be posted on Blackboard.


**Course Outline**

The goal of this course is to introduce students to the field of computer engineering, in particular, the advance topics in digital logic design. Students will develop knowledge of the fundamentals of microprocessor components, information representation, analysis and synthesis of combinational and sequential circuits, datapaths, pipelining, control units, instruction sequencing and interpretations, instruction set architectures and FPGAs. Furthermore, students will develop an awareness of abstraction, computer organization, and software used for the simple digital circuit simulation. Lab work provides hands-on experience with digital systems.

**Course Outcomes**

The primary student outcomes desired for this course listed by topic are:
• An ability to articulate an understanding of the basic microprocessor components and functions, information representation and number arithmetic.

• An ability to analyze and synthesize combinational circuits and sequential circuits using logic gates, K-maps, latches, flip-flops, state tables and state diagrams.

• An ability to analyze and design datapaths (including pipelines, advanced adders, register files, and register transfer language).

• An ability to analyze and design control units (including instruction sequencing and interpretation, timing considerations).

• An ability to demonstrate knowledge of instruction set architectures and their implementation (includes addressing, opcodes and decision making).

• An ability to setup a test procedure for verification of the control units and datapaths implemented on FPGA.

• An ability to analyze and interpret the test and verification of results.

• An ability to implement control units and datapaths on a FPGA using available tools in a laboratory environment.

**Tentative Dates**

**Midterm 1:** May 3, 2010 (in-class)

**Midterm 2:** May 17, 2010 (in-class)

**Final Exam:** June 7, 2010 (10:10 AM - 12:10 PM)